

What is Claimed is:

- [c1] 1. A method of extracting circuit characteristics from a circuit design, said method comprising:
- extracting first cell characteristics from a portion of said circuit design using a first set of environmental conditions;
 - extracting second cell characteristics from said portion of said circuit design using a second set of environmental conditions;
 - determining a difference between said first cell characteristics and said second cell characteristics; and
 - labeling a placeability of said portion of said circuit design based on said difference.
- [c2] 2. The method in claim 1, wherein said circuit characteristics comprise at least one of capacitance, impedance, power, and resistance.
- [c3] 3. The method in claim 1, wherein said first environmental conditions comprise a best environment and said second environmental conditions comprise a worst environment.
- [c4] 4. The method in claim 3, wherein said best environment includes a minimum amount of wiring adjacent said portion of said circuit and said worst environment includes a maximum amount of wiring adjacent said portion of said circuit.
- [c5] 5. The method in claim 1, wherein said labeling of said placeability comprises:
- comparing said difference to a predetermined standard; and
 - labeling said portion of said circuit design as freely placeable within any area of said circuit design if said difference is less than said predetermined standard.
- [c6] 6. A method of extracting circuit characteristics from a circuit design, said method comprising:
- extracting first cell characteristics from a portion of said circuit design using a first set of environmental conditions;
 - extracting second cell characteristics from said portion of said circuit

design using a second set of environmental conditions;
determining a difference between said first cell characteristics and said second cell characteristics;
labeling a placeability of said portion of said circuit design based on said difference; and
replacing said portion of said circuit with a placeholder cell if said portion of said circuit design is freely placeable.

- [c7] 7. The method in claim 6, wherein said circuit characteristics comprise at least one of capacitance, impedance, power, and resistance.
- [c8] 8. The method in claim 6, wherein said first environmental conditions comprise a best environment and said second environmental conditions comprise a worst environment.
- [c9] 9. The method in claim 8, wherein said best environment includes a minimum amount of wiring adjacent said portion of said circuit and said worst environment includes a maximum amount of wiring adjacent said portion of said circuit.
- [c10] 10. The method in claim 6, wherein said labeling of said placeability comprises:
comparing said difference to a predetermined standard; and
labeling said portion of said circuit design as freely placeable within any area of said circuit design if said difference is less than said predetermined standard.
- [c11] 11. The method in claim 6, further comprising calculating average cell characteristics from said portion of said circuit design for said placeholder cell based on an average environment.
- [c12] 12. A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of extracting circuit characteristics from a circuit design, said method comprising:
extracting first cell characteristics from a portion of said circuit design using a first set of environmental conditions;
extracting second cell characteristics from said portion of said circuit

design using a second set of environmental conditions;
determining a difference between said first cell characteristics and said second cell characteristics; and
labeling a placeability of said portion of said circuit design based on said difference.

[c13] 13. The program storage device in claim 12, wherein said circuit characteristics comprise at least one of capacitance, impedance, power, and resistance.

[c14] 14. The program storage device in claim 12, wherein said first environmental conditions comprise a best environment and said second environmental conditions comprise a worst environment.

[c15] 15. The program storage device in claim 14, wherein said best environment includes a minimum amount of wiring adjacent said portion of said circuit and said worst environment includes a maximum amount of wiring adjacent said portion of said circuit.

[c16] 16. The program storage device in claim 12, wherein said labeling of said placeability comprises:
comparing said difference to a predetermined standard; and
labeling said portion of said circuit design as freely placeable within any area of said circuit design if said difference is less than said predetermined standard.

[c17] 17. A method of extracting circuit characteristics from a circuit design, said method comprising:
extracting first cell characteristics from a portion of said circuit design using a first set of environmental conditions;
extracting second cell characteristics from said portion of said circuit design using a second set of environmental conditions;
determining a difference between said first cell characteristics and said second cell characteristics;
comparing said difference to a predetermined standard;
labeling said portion of said circuit design as freely placeable within any

area of said circuit design if said difference is less than said predetermined standard;
replacing said portion of said circuit with a placeholder cell if said portion of said circuit design is freely placeable;
simplifying said placeholder cell in a process comprising:
 shorting all conductors in said portion of said circuit design to a ground node;
 merging all conductors in a given level of said portion of said circuit design;
 removing all conductors that are covered by overlying conductors from said portion of said circuit design; and
 merging conductors outside said portion of said circuit design that are within a predetermined distance to said circuit design with conductors within said portion of said circuit design.

- [c18] 18. The method in claim 17, wherein said circuit characteristics comprise at least one of capacitance, impedance, power, and resistance.
- [c19] 19. The method in claim 17, wherein said first environmental conditions comprise a best environment and said second environmental conditions comprise a worst environment.
- [c20] 20. The method in claim 19, wherein said best environment includes a minimum amount of wiring adjacent said portion of said circuit and said worst environment includes a maximum amount of wiring adjacent said portion of said circuit.
- [c21] 21. The method in claim 17, further comprising calculating average cell characteristics from said portion of said circuit design for said placeholder cell.